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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/777,003	02/05/2001	David Baker	655-0012C	5644

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SOFER & HAROUN, L.L.P.
317 Madison Avenue
Suite 910
New York, NY 10017

EXAMINER	
NGUYEN, TANH Q	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/777,003	BAKER ET AL.	
	Examiner	Art Unit	
	Tanh Q. Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/15/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on November 7, 2005 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of any patent granted on application number 10/867,868 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 41 and 42 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the original specification for "a plurality of modules including an interface unit, which is capable of controlling a first **host** processor". Applicant cited page 15, line 15 as support for such limitation. The cited section does not appear to be sufficient to overcome the rejection, and will be discussed in the "Response to Arguments" section that follows.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 19-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gibson (USP 6,414,687)** in view of **Kusters (USP 5,819,112)**.

6. As per claims 19, 28, **Gibson** teaches an integrated multimedia system [FIG. 1] having a multimedia processor [224, FIG. 1; 224, FIG. 2] disposed in an integrated circuit [ASIC chip: col. 8, lines 66-67], said system comprising:

a first host processor system [202, FIG. 1] coupled to said multimedia processor;

a second local processor [235, FIG. 2] disposed within said multimedia processor for controlling the operation of said multimedia processor [col. 10, line 67-col. 11, line 1];

a data transfer switch [249, 252, FIG. 2] disposed within said multimedia processor and coupled to said second processor for transferring data to various modules of the multimedia processor [235, 236, 238, 246,..., FIG. 2; col. 9, lines 32-36; col. 11, lines 1-9; col. 87, lines 47-50; col. 110, lines 49-51], wherein said data transfer switch is configured to transfer data between said modules of said multimedia processor [col. 9, lines 32-36] in either direction between at least two modules [236, 238 - FIG. 2] within said multimedia processor as requested by said modules [data are received via PCI bus 206, hence via external interface controller 238, and stored in the local memory, hence via the local memory controller 236 [col. 9, lines 8-13]; the input

interface switch 252 transmits data as required to the external interface controller 238 and the local memory controller 236 [col. 110, lines 49-51]; FIG. 2 shows only the external interface controller 238 and the local memory transmitting data to input interface switch 252 - under such conditions the data from the PCI bus is stored in the local memory through path 238-252-236, and under such conditions data transmitted by input interface 252 to external interface controller 238 can only come from local memory controller 236, hence path 236-252-238];

a data streamer [246, 247, 248, 249, 250, FIG. 2] disposed within said multimedia processor and coupled to said data transfer switch, said data streamer having a scheduling logic [811, FIG. 109; col. 78, lines 2-7; col. 77, lines 55-57] that is configured to schedule simultaneous data transfers among a plurality of modules [230/240, 241, 242, 243, 249/236/237/238, 250, 252/236/238, ...FIG. 2] disposed within said multimedia processor, at least one of which is a cache memory [230, FIG. 2] in accordance with corresponding channel allocations [col. 50, lines 50-65; col. 51, lines 40-45; col. 79, lines 4-9; FIGs. 111-114; col. 78, line 32-col. 79, line 3; col. 87, line 40-col. 88, line 48];

an interface unit coupled to said data streamer having a plurality of I/O device driver units [236, 237, 238, 239, FIG. 2]; and

a plurality of external I/O devices [226, 227, Fig. 1] coupled to said multimedia processor.

Gibson, therefore, discloses the invention except for a multiplexer coupled to the interface unit providing access between a selected number of the I/O device driver units

and a plurality of external I/O devices coupled to the multimedia processor via output pins.

Kusters teaches a method that uses a multiplexer [30, FIG. 1] coupled to an interface [18, 20, FIG. 1] of a computer system [8, FIG.1] for providing access between a selected number of I/O device driver units [38a,..,38n, FIG.1] and external I/O devices [32a,..,32n, FIG. 1] via output pins (parallel I/O port, Abstract). Kusters further teaches the above method not being limited to any particular computer, single chip processor or apparatus; and also teaches a specialized apparatus to perform the methods above (col. 8, lines 4-14). Kusters, therefore, teaches a multiplexer being usable with a single chip multimedia processor, such multiplexer being either on the same chip as the multimedia processor, or external to the multimedia processor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a multiplexer disposed within a multimedia processor and coupled the interface of the multimedia processor, as is taught by Kusters for the purpose of providing access between a selected number of I/O device driver units and a plurality of external I/O devices via a limited number of output pins of the multimedia processor - as such combination enables multiple external I/O devices to be used simultaneously with a same set of pins.

7. As per claims 20-27, 29-36, 37-44, Kusters teaches the plurality of external I/O devices [32a,...,32n, FIG. 1] being controlled by a corresponding one of a plurality of device driver units [38a,...,38n, FIG. 1];

Gibson teaches a video coder/decoder [241, FIG. 2] outputting processed data

[col. 9, lines 54-56] to an external I/O device [237, FIG. 2] and receiving data from the external I/O device [237-236-252-246-241, FIG. 2] via the data transfer switch [249, 252, FIG. 2]. Since NTSC is the standard for encoding/decoding color television signal, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a NTSC encoder/decoder as one of the external devices in order to display the picture image in color on a television monitor, and to receive image data from a television monitor;

Kusters teaches one of the external devices being a modem [col. 4, lines 6-9], with modems being known in the art at the time the invention was made to demodulate wireless communications signals, and with a transport channel interface being interface well known in the art at the time the invention was made for modems;

Gibson teaches a video coder/decoder [241, FIG. 2], and an external video display device, hence teaches the multimedia processor providing video signals to the external video display device. Since it was well known in the art at the time the invention was made for multimedia processor to provide 3-D signals to an external video display device, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the ability to provide 3_D signals in the multimedia processor in order to provide 3-D display on the external video display device;

the combination of Gibson and Kusters does not teach one of the external devices being an ISDN interface. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an ISDN interface as one of the

external device in order to allow the multimedia processor to communicate in an ISDN environment, which is superior to a standard telephone line environment;

the combination of Gibson and Kusters does not teach one of the external devices being an audio CODEC. Since it was well known in the art at the time the invention was made for a multimedia processor to communicate with an external audio CODEC, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate an audio CODEC to allow the system to receive and transmit audio signals;

Gibson teaches the cache memory [230, FIG. 2] being directly coupled to the second local processor [235-231, FIG. 2] and the data transfer switch [252-240, FIG. 2];

the interface unit being capable of controlling the external I/O devices (see rejections to claims 19, 28 above), and comprising a memory controller [236, FIG. 2] which is capable of controlling an external memory [223, FIG. 1];

the interface unit comprising an interface which is capable of communicating with the first processor [238, FIG. 2]; and

the data transfer switch comprising a plurality of buses [FIG. 2].

Response to Arguments

8. Applicant's arguments with respect to the 112 rejections of claims 41-42 have been considered but they are not persuasive. The section cited by applicant merely discloses the multimedia processor 100 functioning as either a master or a slave device when coupled to either PCI or AGP bus, and the multimedia processor 100 can operate

as a bus master on one channel and a slave device on the other. The section does not support the host processor operating as a slave of the multimedia processor. Applicant argued that the host system of the PC (corresponding to the first processor) could generally be either a master on the PCI bus or a slave thereof. It appears that applicant merely alleged that the host processor could be a slave without providing support for such allegation.

9. Applicant's arguments with respect to - transfer of data in either direction between at least two modules within the multimedia processor as requested by said modules - are moot in view of the new ground(s) of rejection.

10. Applicant's arguments with respect to Kusters have been fully considered but they are not persuasive.

Applicant argued that Kusters does not contain a data transfer switch similar to that of the present invention, that the present invention allows access between the plurality of I/O devices and a selected number of I/O device driver units, and that Kusters does not teach a multiplexer analogous to the multiplexer of the present invention.

Kusters was not relied upon to teach a data transfer switch. It appears that applicant, in making the argument with respect to the data transfer switch, is attacking the references individually and/or arguing bodily incorporation. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA

1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

It is further noted that the invention, as claimed, does not preclude Kusters' teachings (see Kusters' teaching in the rejections). Applicant merely alleged that Kusters' multiplexer is not analogous to the multiplexer of the present invention, but does not point how the language of the claims patentably distinguishes them from the references. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Quang Nguyen whose telephone number is (571) 272-4154 and whose e-mail address is tanh.nguyen36@uspto.gov. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh, can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300 for After Final, Official, and Customer Services, or (571) 273-4154 for Draft to the Examiner (please label "PROPOSED" or "DRAFT").

Effective May 1, 2003 are new mailing address is:

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01/23/2006

TQN
January 23, 2006